HOST TO FPGA INTERFACE IN AN IN-CIRCUIT EMULATION SYSTEM

ABSTRACT OF THE DISCLOSURE

A multi-purpose interface between a host computer and an FPGA. This interface uses an IEEE 1284 compliant EPP mode connection. When the host computer is initialized, a reset of the FPGA is carried out to clear the configuration memory of the FPGA. The data lines of the interface are then used to communicate unidirectional configuration data into the FPGA. The data are clocked by the host computer using the data strobe signal line to clock data into the FPGA. When the FPGA has been fully programmed, including programming an IEEE 1284 compliant EPP mode interface into the FPGA, the data lines are used for bidirectional communication between the host computer and the configured FPGA, in this embodiment operating as a virtual microcontroller.